

WHAT IS CLAIMED IS:

1 1. A method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system comprising:
3 transmitting a first digital signal along the first signal path;
4 transmitting a second digital signal along the second signal path wherein the second
5 digital signal has a value opposite a value of the first digital signal;
6 inverting the value of the first digital signal along the first signal path to match the
7 value of second digital signal; and
8 re-inverting the first digital signal along the first signal path at a final destination of
9 the first signal path.

1 2. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 1 further comprising:
3 storing the second signal in a buffer along the second signal path.

1 3. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 2 wherein inverting the
3 first digital signal takes place when storing the second signal.

1 4. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 1 further comprising:
3 repeating the first digital signal along the first path; and
4 repeating the second digital signal along the second path.

1 5. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 2 further comprising:
3 a first signal repeater that repeats the first digital signal after the first digital signal is
4 inverted; and
5 a second signal repeater that repeats the second digital signal after the second digital
6 signal is stored.

1 6. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 1 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 7. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 2 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 8. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 3 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 9. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 4 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 10. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 5 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 11. The method of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 6 wherein
3 the value of the first digital signal and the value of the second digital signal are the
4 same for at least one half of the first signal path.

1 12. An electrical transmission circuit comprised of:
2 a sending device transmitting a first digital signal having a value along a first signal
3 path;
4 a second device transmitting a second digital signal having a value opposite the value
5 of the first digital signal along a second signal path;
6 an inverter device that inverts the value of the first digital signal to match the value of
7 the second digital signal; and
8 a receiving device that receives the first digital signal and the second digital signal
9 wherein the receiving device inverts the value of the first digital signal.

1 13. The electrical transmission circuit of claim 12 further comprised of:
2 a buffer device along the second signal path that stores the value of the second digital
3 signal.

1 14. The electrical transmission circuit of claim 13 wherein the inverter is placed
2 opposite the buffer device.

1 15. The electrical transmission circuit of claim 12 further comprised of:
2 a first repeater device that repeats the first digital signal along the first signal path;
3 and
4 a second repeater device that repeats the second digital signal along the second signal
5 path.

1 16. The electrical transmission circuit of claim 13 further comprised of:
2 a first repeater device that repeats the first digital signal after the first digital signal is
3 inverted; and
4 a second repeater devices that repeats the second digital signal after the second digital
5 signal is stored.

1 17. The electrical transmission circuit of claim 12 wherein the value of the first
2 digital signal and the value of the second digital signal are the same for at least one half of the
3 first signal path.

1 18. The electrical transmission circuit of claim 13 wherein the value of the first
2 digital signal and the value of the second digital signal are the same for at least one half of the
3 first signal path.

1 19. The electrical transmission circuit of claim 14 wherein the value of the first
2 digital signal and the value of the second digital signal are the same for at least one half of the
3 first signal path.

1 20. The electrical transmission circuit of claim 15 wherein the value of the first
2 digital signal and the value of the second digital signal are the same for at least one half of the
3 first signal path.

1 21. The electrical transmission circuit of claim 16 wherein the value of the first
2 digital signal and the value of the second digital signal are the same for at least one half of the
3 first signal path.

1 22. An apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system comprised of:
3 means for transmitting a first digital signal along the first signal path;
4 means for transmitting a second digital signal along the second signal path wherein
5 the second digital signal has a value opposite a value of the first digital signal;
6 means for inverting the value of the first digital signal along the first signal path to
7 match the value of second digital signal; and
8 means for re-inverting the first digital signal along the first signal path at a final
9 destination of the first signal path.

1 23. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 22 further comprised of:
3 means for storing the second digital signal in a buffer along the second signal path.

1 24. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 23 wherein the means for
3 inverting the first digital signal takes place when storing the second digital signal.

1 25. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 22 further comprised of:
3 means for repeating the first digital signal; and
4 means for repeating the second digital signal.

1 26. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 23 further comprised of:
3 means for repeating the first digital signal after inverting the first digital signal; and
4 means for repeating the second digital signal after storing the second digital signal.

1 27. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 22 wherein the value of
3 the first digital signal and the value of the second digital signal are the same for at least one
4 half of the first signal path.

1 28. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 23 wherein the value of
3 the first digital signal and the value of the second digital signal are the same for at least one
4 half of the first signal path.

1 29. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 24 wherein the value of
3 the first digital signal and the value of the second digital signal are the same for at least one
4 half of the first signal path.

1 30. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 25 wherein the value of
3 the first digital signal and the value of the second digital signal are the same for at least one
4 half of the first signal path.

1 31. The apparatus of minimizing coupling capacitance interference between a first
2 signal path and a second signal path in an electrical system of claim 26 wherein the value of
3 the first digital signal and the value of the second digital signal are the same for at least one
4 half of the first signal path.